UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,303	12/03/2001	Sung-Chan Park	08244.0032	4821

7590 05/19/2003

Finnegan, Henderson, Farabow,
Garrett & Dunner, L.L.P.
1300 I Street, N.W.
Washington, DC 20005-3315

EXAMINER	
NGUYEN, THANH T	
ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 05/19/2003

8

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/998,303	Applicant(s) PARK ET AL.	
	Examiner Thanh T. Nguyen	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

Claims 1-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation "forming insulating layers on sidewalls of the bit line patterns" is indefinite because it is unclear how the insulating layers forming on the sidewalls of the bit line patterns without exposing the bit line patterns first. It is suggested to add the limitation "wherein etching to expose sidewall of the bit line patterns" at the end of step "c".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by the Admitted Prior Art (figures 2a-7D, Pages 1-7).

Regarding to claim 1, Referring to figures 2a-7D, the Admitted Prior Art teaches a method for forming contact openings (10, called contact hole) between bit line patterns (21A) the method comprising the steps of:

a) forming bit line patterns (21A) on a substrate (20) including word line patterns (WL, see figure 5) thereby forming a first resulting structure,

b) forming an interlayer insulating layer (25, oxide, as claimed in claim 3) on the first resulting structure (see figure 2D),

c) etching the interlayer with an etching mask (26, photoresist mask) (see figure 2E), and forming a contact opening (10) between neighboring bit line patterns (21A), and

d) forming insulating layers (24) on the side wall of the bit line patterns (21A).

Regarding to claim 6, wherein top surfaces of the bit line patterns are covered with a layer selected from a group consisting of a silicon nitride layer (see page 2, lines 1-2, Noted that silicon nitride layer can be called nitride layer)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art (figures 2a-7D, Pages 1-7) and further in view of cooper et al. (U.S. Patent No. 5,219,793).

Regarding to claim 1, Referring to figures 2a-7D, the Admitted Prior Art teaches a method for forming contact openings (10, called contact hole) between bit line patterns (21A) the method comprising the steps of:

a) forming bit line patterns (21A) on a substrate (20) including word line patterns (WL, see figure 5) thereby forming a first resulting structure,

b) forming an interlayer insulating layer (25, oxide, as claimed in claim 3) on the first resulting structure (see figure 2D),

c) etching the interlayer with an etching mask (26, photoresist mask) (see figure 2E), and forming a contact opening (10) between neighboring bit line patterns (21A), and

d) forming insulating layers (24) on the side wall of the bit line patterns (21A).

Regarding to claim 6, wherein top surfaces of the bit line patterns are covered with a layer selected from a group consisting of a silicon nitride layer (see page 2, lines 1-2, Noted that silicon nitride layer can be called nitride layer)

However, the Admitted Prior Art does not teach the interlayer insulating layer has a low dielectric constant is etched a gas mixture of CF_4, CHF_3, and argon (Ar) or using a gas selected from Ar, O_2, N_2, H_2, CH_4, C_2H_4 and C_xF_y as claimed in claims 2-4, 8. Nevertheless, such processing step is known in the semiconductor processing art as evidenced by Cooper et al.. Cooper teaches forming an oxide interlayer insulating layer (18) and SOG layer (22, spin on glass, Noted SOG layer is a low dielectric oxide layer which has the dielectric constant less than

3.5 as claimed in claims 2-3) is etched with a mixture of CF_4, CHF_3, and argon (Ar) or one of Ar, O_2 and C_2F_6, at the pressure of 150-350 mtorr (see col. 5, lines 4-19). It would have been obvious to a person of ordinary skill in the art at the time of the invention was made would have used a mixture of CF_4, CHF_3, and argon (Ar) or one of Ar, O_2 and C_2F_6 to etch the interlayer insulating layer in the Admitted Prior Art's process as taught by Cooper et al. ***because*** carbon and fluorine compound plasma can selectively etch the oxide interlayer insulating layer and remove all the oxide interlayer layer to expose the contact region between conductive patterns, and in the case when some spacing between conductive patterns wider than the other, the carbon and fluorine compound plasma can selectively etch the oxide interlayer insulating layer and leave a portion of oxide interlayer insulating layer on the sidewall of the conductive patterns to form sidewall spacers and also expose the contact region between the conductive patterns.

Regarding to claim 6, method of forming a mask pattern covering a top portion of the conductive layer pattern wherein the mask pattern is formed of a layer selected from a group consisting of silicon nitride. Nevertheless, such processing step is known in the semiconductor processing art as evidenced by Cooper. Cooper teaches forming a mask pattern (16) covering a top portion of the conductive layer pattern (14) wherein the mask pattern (16) is formed of a layer selected from a group consisting of silicon nitride (see figure 1 and col. 3, lines 52-63). It would have been obvious to a person of ordinary skill in the art at the time of the invention was made would have formed a silicon nitride mask pattern covering a top portion of the conductive layer pattern in the Admitted Prior Art's process as taught by Cooper et al. ***because*** the silicon nitride mask pattern provides protection to the top surface of conductive layer pattern during the

etching process of interlayer insulating layer, so that the top surface of the conductive layer pattern can not be etched or damaged by the chemical or plasma.

Regarding to claims 5, 9, the specific etching pressure range as claimed are taken to be obvious since these are variables of art recognized importance which are subject to routine experimentation and optimization and discovery of an optimum value for a known process is obvious. In re Aller, 105 USPQ 233 (CCPA 1955). And, even if applicants' modification results in great improvement and utility over the prior art, it may still not be patentable if the modification was within the capabilities of one skilled in the art, In Re Sola 25 USPQ 433. Since, Cooper teaches that the oxide interlayer insulating layer (18, 22) is etched with a mixture of CF_4, CHF_3, and argon (Ar) or one of Ar, O_2 and C_2F_6 at the pressure of 150-350 mtorr (see col. 5, lines 4-19), hence, one of ordinary skill in the requisite art at the time the invention was made would have adjusted the plasma etching pressure to the range of less than 100 mtorr to etch the interlayer insulating layer ***because*** when an optimum etching pressure in the etching chamber is used to etch the interlayer insulating layer, the interlayer insulating layer in the contact region can be completely removed or at the same time leaving a portion of the interlayer insulating layer on the sidewall of conductive layer patterns depending on the spacing between the conductive layer patterns.

Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art (figures 2a-7D, Pages 1-7), and further in view of Chang et al. (U.S. Patent No. 6,159,842) and further in view of Tsai et al. (U.S. Patent No. 6,331,480).

Regarding to claim 7, the interlayer insulating layer is formed of a polymer. Nevertheless, such processing step is known in the semiconductor processing art as evidenced by Chang et al. Chang et al. teaches forming a low dielectric constant material layer HSQ layer (18) having a dielectric constant about 3 over the conductive layer patterns (14) (see figure 1 and col. 4, lines 22-40). The HSQ layer is a silicon polymer and spin-on insulating oxide material having a dielectric constant of 2.7-3.0 (see col. 1, lines 50-55). It would have been obvious to a person of ordinary skill in the art at the time of the invention was made would have used a silicon polymer HSQ layer having low dielectric constant to replace the Admited Prior Art's low dielectric interlayer insulating layer as taught by Chang et al. ***because*** silicon polymer HSQ layer can be easily deposited over the conductive layer patterns by spin-on coating process, and HSQ material also has the same low dielectric constant characteristics as the other low dielectric constant material which eliminates the capacitive interaction or coupling between closely-spaced conductive layer patterns.

Regarding to claim 8, the interlayer insulating layer is formed of a polymer and etched with a gas selected from Ar, O_2, N_2, H_2, CH_4, C_2H_4 and C_xF_y. Nevertheless, such processing step is known in the semiconductor processing art as evidenced by Tsai et al. Tsai et al. teaches etching low dielectric constant material HSQ having a dielectric constant of about 2.5-3.5 with an etchant of O_2/C_2F_6 (see col. 3, lines 15-21).

Since, Chang et al. teaches forming a low dielectric constant material layer of polymer HSQ layer over the conductive layer patterns having a dielectric constant of 2.7-3.0. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made

would have etched a silicon polymer HSQ layer with an etchant of O_2/C_2F_6 in Chang et al.'s process as taught by Tsai et al. ***because*** Chang et al. and Tsai et al. both have similar HSQ material, and HSQ material layer which can be selectively etched with O_2 and/or C_2F_6 to form spacers on the sidewall of conductive layer pattern and/or expose the conductive region.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (703) 308-9439, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:30AM to 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (703) 308-4940. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).

Thanh Nguyen

Carl Whitehead

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

15 May 2003